2019 NSE Grantees Conference

Creating Novel NanoSystems to Enable Artificial Intelligence

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Abstract: The world's appetite for analyzing massive amounts of data (streaming video and audio, natural languages, real-time sensor readings, contextual environments or even brain signals) is growing dramatically. The computation demands of these abundant-data applications, such as machine learning, far exceed the capabilities of today's computing systems, and can no longer be met by isolated improvements in transistor technologies, memories or integrated circuit architectures alone. To achieve unprecedented functionality, speed and energy efficiency, one must create transformative NanoSystems which exploit unique properties of underlying nanotechnologies to implement new architectures.

This talk will present the *N3XT* (Nano-Engineered Computing Systems Technology) approach that enables such NanoSystems through: (i) new computing system architectures leveraging emerging device (logic and memory) nanotechnologies and their dense 3D integration with fine-grained connectivity for computation immersed in memory, (ii) new logic devices (such as carbon nanotube field-effect transistors for implementing high-speed and low-energy logic circuits) as well as high-density non-volatile memory (such as resistive RAM that can store multiple bits inside each memory cell), amenable to (iii) ultra-dense (monolithic) 3D integration of thin layers of logic and memory devices that are fabricated at a low temperature.

A wide variety of *N3XT* hardware prototypes (built in research facilities and also in US foundry as part of DARPA's 3DSoC program) represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual NanoSystems. *N3XT* NanoSystems target 1,000X system-level energy-delay product benefits especially for abundant-data applications. Such massive benefits enable a wide range of applications that push new frontiers, from deeply-embedded computing systems all the way to the cloud.

Bio: Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, co-leads the Computation focus area of the Stanford SystemX Alliance, and is a faculty member of the Wu Tsai Neurosciences Institute. Prof. Mitra also holds the Carnot Chair of Excellence in NanoSystems at CEA-LETI in Grenoble, France. His research ranges across robust computing, NanoSystems, Electronic Design Automation, and neurosciences. Results from his research group have been widely deployed by

industry and have inspired significant development efforts by government and research organizations in multiple countries.

Jointly with his students and collaborators, Prof. Mitra demonstrated the first carbon nanotube computer and the first three-dimensional NanoSystem with computation immersed in data storage. These demonstrations received wide-spread recognition: cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, and highlight as "important, scientific breakthrough" by news organizations around the world.

In the field of robust computing, Prof. Mitra and his students created key approaches for soft error resilience, circuit failure prediction, on-line self-test and diagnostics, and QED (Quick Error Detection) design verification and system validation. His earlier work on X-Compact test compression at Intel Corporation has proven essential to cost-effective manufacturing and high-quality testing of almost all electronic systems across the industry. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools.

Prof. Mitra's honors include the ACM SIGDA / IEEE CEDA Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation's Technical Excellence Award (for innovation that significantly enhances the semiconductor industry), the Intel Achievement Award (Intel’s highest corporate honor), and the United States Presidential Early Career Award for Scientists and Engineers from the White House. He and his students have published award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, ACM/IEEE International Conference on Computer-Aided Design, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford."

Prof. Mitra has served on the Defense Advanced Research Projects Agency's (DARPA) Information Science and Technology Board as an invited member. He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).